F3 cont

protection element 32, the N^+ diffusion layer 74 connected to the ground potential wire 12, and the N^+ diffusion layer 76 is connected to the input/output terminal 30. As shown in Fig. 9, a wire 34 to the internal circuit 20 is connected to the input/output terminal 30 in addition to the electrostatic protection element 32.

IN THE CLAIMS:

Please enter the following amended claims:

G1

30. (*Amended*) The semiconductor integrated circuit device according to claim 1, wherein said electrostatic protection element is a bipolar transistor.

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31. (*Amended*) The semiconductor integrated circuit device according to claim 1, wherein said electrostatic protection element is a thyristor.

32. (*Amended*) The semiconductor integrated circuit device according to claim 1, wherein said electrostatic protection element is a diode.